3. (Original) The flash memory of claim 1 further comprising input circuitry to receive input data on the data connections on rising and falling edges of ~~a~~ the clock signal.

B1 cont

4. (currently amended) A flash memory comprising:

an array of non-volatile memory cells;

~~data connections;~~

a clock signal connection to receive a clock signal;

~~an interconnect configuration compatible with~~ a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented;

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal; and

input circuitry to receive input data on the data connections on rising and falling edges of the clock signal.

Claims 5-13 (cancelled)

14. (Previously added) The flash memory of claim 1, wherein the array of non-volatile memory cells are arranged in a plurality of addressable banks.

15. (Previously added) The flash memory of claim 14, wherein each addressable bank contains addressable sectors of memory cells.

16. (Previously added) The flash memory of claim 1, wherein the output circuitry is adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

17. (Previously added) The flash memory of claim 4, wherein the output circuitry is further

adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

Bl Conc'd

18. (currently amended) A flash memory comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks;

~~data connections;~~

a clock signal connection to receive a clock signal;

~~an interconnect configuration compatible with~~ a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented;

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal;

input circuitry to receive input data on the data connections at a rate of two data words per clock cycle; and

sense amplifier circuitry coupled to the array, wherein the sense amplifier circuitry detects a differential voltage.

19. (Previously added) The flash memory of claim 18, wherein the memory is adapted to provide burst-oriented read accesses.